WE CLAIM:

1. A method of processing data in a bi-directional processing device, the method comprising:

(a) receiving said data by a first processor from a bi-directional interface, said first processor operative to perform a first task on said data thereby resulting in processed data;

(b) storing said processed data in a shared memory by said first processor;

(c) retrieving said processed data from said shared memory by a second processor operative to perform a second task on said data; and

(d) transmitting, selectively, said processed data to said bi-directional interface from said second processor.

2. The method of Claim 1, wherein said shared memory comprises first and second banks, wherein one of said first and second banks is accessible to said first processor at substantially all times and the other is accessible to said second processor at substantially all times, said method further comprising:

(e) mirroring data stored by said first processor in one said first and second banks to the other of said first and second banks.

3. The method of Claim 1, wherein said first task comprises at least one of inspection and analysis.

4. The method of Claim 1, wherein said second task comprises taking an action.

5. The method Claim 4, wherein said taking an action comprises at least one of deleting, modifying and transmitting said data.

6. The method of Claim 1, wherein each of said first and second processors are characterized by a bi-directional bandwidth, said method further comprising utilizing substantially all of said bi-directional bandwidth for uni-directional data flow.

7. The method of Claim 1, wherein said storing further comprises storing said processed data such that said second processor is unaware of how said processed data was stored in said shared memory.

8. The method of Claim 1, wherein said method further comprises using first and second processors which comprise network processors.

9. The method of Claim 1, wherein said transmitting is further based on a result of said second task.

10. A bi-directional data processor comprising:

a first processor coupled with a bi-directional interface and operative to receive data from said bi-directional interface and perform a first task on said data thereby resulting in processed data;

a shared memory coupled with said first processor, wherein said first processor is further operative to store said processed data in said shared memory; and

a second processor coupled with said shared memory and said bi-directional interface, said second processor operative to retrieve said stored processed data from said shared memory, perform a second task on said stored processed data thereby resulting in secondarily processed data and selectively transmit said secondarily processed data back to said bi-directional interface.

11. The bi-directional data processor of Claim 10, wherein said shared memory comprises first and second banks, wherein one of said first and second banks is accessible to said first processor at substantially all times and the other is accessible to said second processor at substantially all times, said bi-directional data processor further comprising:

mirroring logic coupled with said first processor and said first and second banks and operative to mirror said processed data stored by said first processor in one of said first and second banks to the other of said first and second banks.

12. The bi-directional data processor of Claim 10, wherein said first task comprises at least one of inspection and analysis.

13. The bi-directional data processor of Claim 10, wherein said second task comprises taking an action.

14. The bi-directional data processor Claim 13, wherein said taking an action comprises at least one of deleting, modifying and transmitting said data.

15. The bi-directional data processor of Claim 10, wherein each of said first and second processors are characterized by a bi-directional bandwidth, substantially all of said bi-directional bandwidth being utilized for uni-directional data flow.

16. The bi-directional data processor of Claim 10, wherein said second processor is unaware of how said processed data was stored in said shared memory.

17. The bi-directional data processor of Claim 10, wherein said first and second processors comprises network processors.

18. The bi-directional data processor of Claim 10, wherein said selective transmission by said second processor is further based on a result of said second task.

19. An apparatus for processing a bi-directional dataflow comprising:

first processor means for receiving data from a bi-directional interface and performing a first task on said data;

shared memory means coupled with said first processor, wherein said first processor is further operative to store said processed data in said shared memory means; and

second processor means coupled with said shared memory and operative to retrieve said stored processed data from said shared memory, perform a second task on said data and selectively transmit said data back to said bi-directional interface.